WE CLAIM:

1. A system for automatically detecting a baud rate of an asynchronous serial bit stream during an initial setup phase comprising:

a predefined data set received from a transmitter;

a transition detector for identifying bit transitions in the predefined data set;

a timer triggered by said transition detector measuring a time interval between two predefined bit transitions;

a storage element for registering the measured time interval; and

a look up table accessible for determining a nearest baud rate value corresponding to the registered time interval.

2. The system of claim 1, wherein the predefined data set is the "ENTER" character of the ASCII code.

3. The system of claim 1, wherein the predefined bit transitions define a measured time interval having the longest duration between two of the identified bit transitions.

4. The system of claim 1, wherein the predefined bit transitions exclude a start bit.

5. A microcomputer system for automatically detecting a baud rate of an asynchronous serial bit stream received from a transmitter during an initial startup phase, comprising:

an interrupt generator triggered by two consecutive bit transitions of the received bit stream,

a timer triggered by the interrupt generator measuring a time interval between the bit transitions, and

a look up table defining baud rates for a set of time intervals, the table being accessible to compare the measured time interval to the set of time intervals to determine a nearest baud rate corresponding to said measured time interval.

6. The microcomputer system of claim 5, wherein the received bit stream includes a predefined data set comprising an "ENTER" character of the ASCII code.

7. The microcomputer system of claim 5, wherein said predefined bit transitions correspond to the longest duration between bit transitions.

8. A microcomputer system as claimed in claim 5 wherein the bit transitions exclude the start bit.

9. A method for automatically detecting a baud rate of a bit stream during, comprising:

receiving a bit stream comprising a data set,

measuring a time interval between two bit transitions in the data set, and

selecting a nearest baud rate corresponding to the measured time interval from a look-up table.

10. The method of claim 9, wherein the data set comprises the "ENTER" character of the ASCII code.

11. The method of claim 9, wherein the bit transitions correspond to a longest duration transition interval in the bit stream.

12. The method of claim 9, wherein the bit transitions exclude an initial bit transition corresponding to a start bit.

13. A computer readable medium for automatic baud rate detection, comprising:

computer readable program code devices configured to cause a microcontroller to toggle a compare register bit value on interrupts generated by an I/O port of the microcontroller, whereby interrupts are edge triggered;

computer readable program code devices configured to cause the microcontroller to initialise a timer counter to count a time period between two interrupts;

computer readable program code devices configured to cause the microcontroller to receive a known data set from a transmitter;

computer readable program code devices configured to cause the microcontroller to detect transition timings corresponding to a predetermined part of the data set to compute a transition time between two transitions indicated by the interrupts; and

computer readable program code devices configured to cause the microcontroller to select a baud rate corresponding to the transition time for use in configuring the microcontroller.

14. The computer readable medium of claim 13, wherein the two transitions are selected to have a longest duration of pairs of transitions in the known data set.

15. The computer readable medium of claim 13, wherein the known data set includes a synchronizing character from the transmitter.

16. The computer readable medium of claim 15, wherein the synchronizing character is the "ENTER" character of the ASCII code.

17. The computer readable medium of claim 13, further including computer readable program code devices configured to cause the microcontroller to set the I/O port to a compare mode to generate an interrupt when an input signal differs from the compare register bit value.